WHAT IS CLAIMED IS:

1. A semiconductor bare chip having an integrated circuit formed on front surface thereof, wherein a magnetic loss film is formed on back surface of said semiconductor bare chip.

2. The semiconductor bare chip according to claim 1, wherein said magnetic loss film is a granular magnetic thin film.

3. The semiconductor bare chip according to claim 2, wherein said granular magnetic thin film is a sputtered film formed by a sputtering method.

4. The semiconductor bare chip according to claim 2, wherein said granular magnetic thin film is a vapor-deposited film formed by a vapor deposition method.

5. A semiconductor wafer having an integrated circuit formed on front surface thereof,
wherein a magnetic loss film is formed on back surface of said semiconductor wafer.

6. The semiconductor wafer according to claim 5, wherein said magnetic loss film is a granular magnetic thin film.

7. The semiconductor wafer according to claim 6, wherein said granular magnetic thin film is a sputtered film formed by a sputtering method.

8. The semiconductor wafer according to claim 6, wherein said granular magnetic thin film is a vapor-deposited film formed by a vapor deposition method.

9. A semiconductor substrate having a magnetic loss member formed in a part thereof, wherein

said magnetic loss member is formed in a prescribed pattern in vicinity of the surface on one side of said semiconductor substrate; and
said magnetic loss member and semiconductor substrate region on said surface

are uniformly covered with an insulating film.

10. The semiconductor substrate according to claim 9, wherein said magnetic loss member is formed over substantially entire surface of said semiconductor substrate.

11. The semiconductor substrate according to claim 9, wherein said prescribed pattern is formed by said magnetic loss member and is a striped pattern.

12. The semiconductor substrate according to claim 9, wherein said prescribed pattern is formed by said magnetic loss member and is a lattice pattern.

13. The semiconductor substrate according to claim 9, wherein said prescribed pattern is formed by said magnetic loss member and is an island pattern.

14. The semiconductor substrate according to claim 9, wherein said insulating film comprises at least one material selected from a group consisting of silicon oxide, silicon nitride, and silicon nitride oxide.

15. A semiconductor substrate having a plurality of magnetic loss members formed in a part thereof, wherein said magnetic loss members are formed in a prescribed pattern, each of said magnetic loss members being formed on an inside surface of each semiconductor device region which is separated by dividing said semiconductor substrate.

16. A semiconductor substrate formed by joining a first semiconductor substrate member and a second semiconductor substrate member together, and having a magnetic loss member formed in a part thereof, wherein

at least one semiconductor substrate member of said first semiconductor substrate member and said second semiconductor substrate member is provided with a trench, which is formed on the surface thereof that is joined together; and

said magnetic loss member is embedded inside said trench.

17. The semiconductor substrate according to claim 16, wherein said trench comprises a plurality of trench portions formed in a prescribed pattern, each of said trench portions being formed on an inside surface of each semiconductor device region which is separated by dividing said semiconductor substrate.

18. The semiconductor substrate according to claim 16 wherein said magnetic loss member is composed of M-X-Y, where M is either any one of, or a mixture of, Fe, Co, and Ni, X is either an element other than M and Y, or a mixture thereof, and Y is any one of, or a mixture of, F, N, and O.

19. The semiconductor substrate according to claim 9, wherein material of the semiconductor substrate, said first semiconductor substrate member, and said second semiconductor substrate member, respectively, consists of silicon.

20. The semiconductor substrate according to claim 9, wherein material of the semiconductor substrate, said first semiconductor substrate member, and said second semiconductor substrate member, respectively, consists of gallium-arsenic.

21. A plurality of semiconductor devices that is repeatedly formed in a prescribed pattern on the semiconductor substrate according to claim 9, wherein:

each of said plurality of semiconductor devices comprises at least one unit region in which said magnetic loss member is formed.

22. A semiconductor substrate manufacturing method comprising a process for forming a layer comprising a magnetic loss member in at least a part of said semiconductor substrate.

23. The semiconductor substrate manufacturing method according to claim 22, wherein said magnetic loss member is composed of M-X-Y, where M is either any one of, or a mixture of, Fe, Co, and Ni, X is either an element other than M and Y, or a mixture thereof, and Y is any one of, or a mixture of, F, N, and O.

24. The semiconductor substrate manufacturing method according to claim 22, wherein material of the semiconductor substrate, said first semiconductor substrate member, and said second semiconductor substrate member, respectively, consists of silicon.

25. The semiconductor substrate manufacturing method according to claim 9, wherein material of the semiconductor substrate, said first semiconductor substrate member, and said second semiconductor substrate member, respectively, consists of gallium-arsenic.

26. The semiconductor substrate manufacturing method according to claim 22, comprising:

a first process for forming said magnetic loss member or members on the surface on one side of said semiconductor substrate, in a prescribed pattern, with a prescribed film thickness; and

a second process for uniformly coating entire surface of said semiconductor substrate, inclusive of said magnetic loss member or members, with an insulating film, subsequent to said first process.

27. The semiconductor substrate manufacturing method according to claim 22, comprising fabrication of a semiconductor substrate by forming a trench structure or structures in at least said first semiconductor substrate member, and attaching said second semiconductor substrate member to said first semiconductor substrate member after forming said magnetic loss member or members inside said trench structure or structures; said manufacturing method comprising the steps of:

forming an insulating film pattern on said first semiconductor substrate member;

forming said trench structure or structures to a prescribed depth by subjecting said first semiconductor substrate member to an etching process after forming said insulating film pattern;

removing said insulating film pattern from said first semiconductor substrate member after forming said trench structure or structures;

uniformly forming a film of said magnetic loss member on said first semiconductor substrate member after removing said insulating film pattern;

subjecting the entire surface of said first semiconductor substrate member to a polishing treatment so that substrate surface in the regions other than those of said trench structure or structures is exposed, after forming the film of magnetic loss member; and

bringing said second semiconductor substrate member into tight contact with said first semiconductor substrate member subjected to said polishing treatment and performing an adhesive joining process.

28. The semiconductor substrate manufacturing method according to claim 22, comprising fabrication of a semiconductor substrate by forming a trench structure or structures in at least said first semiconductor substrate member, and joining said second semiconductor substrate member to said first semiconductor substrate member after forming said magnetic loss member or members inside said trench structure or structures; said manufacturing method comprising the steps of:

forming an insulating film pattern on said first semiconductor substrate member;

forming said trench structure or structures to a prescribed depth by subjecting said first semiconductor substrate member to an etching process, after forming said insulating film pattern;

removing said insulating film pattern from said first semiconductor substrate member after forming said trench structure or structures;

uniformly forming a film of said magnetic loss member on said first semiconductor substrate member after removing said insulating film pattern;

subjecting the ntire surface of said first semiconductor substrate member to a polishing treatment so that substrate surface in the regions other than those of said trench structure or structures is exposed, after forming said film of magnetic loss member;

thermally oxidizing the entire surface of said second semiconductor substrate member, in which said trench structure or structures are not formed, that opposes said first semiconductor substrate member; and

joining said second semiconductor substrate member, the opposing surface of which was thermally oxidized, to said first semiconductor substrate member, by means of electrostatic bonding.

29. An electromagnetic noise suppression body comprising an electrically conductive soft magnetic thin film; and having a structure, wherein said soft magnetic thin film is finely divided into configuring units sufficiently small relative to wavelength of electromagnetic noise; and

conduction of DC current between those configuring units is interrupted.

30. The electromagnetic noise suppression body according to claim 29, wherein said soft magnetic thin film has an aspect ratio of 10 or greater.

31. The electromagnetic noise suppression body according to claim 29, wherein said soft magnetic thin film is composed of a composition of M-X-Y, where M is either any one of, or a mixture of, Fe, Co, and Ni, X is either an element other than M and Y, or a mixture thereof, and Y is any one of, or a mixture of, F, N, and O, and has a granular structure.

32. A electromagnetic noise suppression method, wherein conductive electromagnetic noise is suppressed by forming said electromagnetic noise

suppression body immediately above a microstrip line or signal transmission line similar thereto.

33. The electromagnetic noise suppression method according to claim 32, wherein said electromagnetic noise suppression body is attached so that the axis of hard magnetization thereof is substantially parallel to the width direction of said microstrip line or signal transmission line similar thereto.

34. The electromagnetic noise suppression method according to claim 32, wherein said soft magnetic thin film is composed of a composition of M-X-Y, where M is either any one of, or a mixture of, Fe, Co, and Ni, X is either an element other than M and Y, or a mixture thereof, and Y is any one of, or a mixture of, F, N, and O, and has a granular structure.

35. An electromagnetic noise suppression body for suppressing conductive electromagnetic noise, comprising an electrically conductive soft magnetic thin film attached in vicinity above a microstrip line or signal transmission line similar thereto, wherein said electrically conductive soft magnetic thin film is of a shape having a width that is substantially equivalent to or narrower than line width of said microstrip line or signal transmission line similar thereto.

36. The electromagnetic noise suppression body according to claim 35, wherein said electromagnetic noise suppression body is attached so that the axis of hard magnetization thereof is substantially parallel to the width direction of said microstrip line or signal transmission line similar thereto.

37. The electromagnetic noise suppression body according to claim 35, wherein said soft magnetic thin film of a shape having a width that is substantially equivalent to or narrower than line width of said microstrip line or analogous signal transmission line has an aspect ratio in width direction of 10 or greater.

38. The electromagnetic noise suppression body according to claim 35, wherein said soft magnetic thin film is composed of a composition of M-X-Y, where M is either any one of, or a mixture of, Fe, Co, and Ni, X is either an element other than M and Y, or a mixture thereof, and Y is any one of, or a mixture of, F, N, and O, and has a granular structure.

39. A conductive noise suppression method for suppressing conductive electromagnetic noise by forming an electromagnetic noise suppression body comprising an electrically conductive soft magnetic thin film in vicinity above a microstrip line or signal transmission line similar thereto, wherein

said electrically conductive soft magnetic thin film is shaped such that a width thereof is substantially equivalent to or narrower than line width of said microstrip line or signal transmission line similar thereto.

40. The electromagnetic noise suppression method according to claim 39, wherein said electromagnetic noise suppression body is attached so that the axis of hard magnetization thereof is substantially parallel to the width direction of said microstrip line or signal transmission line similar thereto.

41. The electromagnetic noise suppression method according to claim 39, wherein said soft magnetic thin film has a shape having a width that is substantially equivalent to or narrower than line width of said microstrip line or analogous signal transmission line and has an aspect ratio is 10 or greater in width direction.

42. The electromagnetic noise suppression method according to claim 39, wherein said soft magnetic thin film is composed of a composition of M-X-Y, where M is either any one of, or a mixture of, Fe, Co, and Ni, X is either an element other than M and Y, or a mixture thereof, and Y is any one of, or a mixture of, F, N, and O, and has a granular structure.